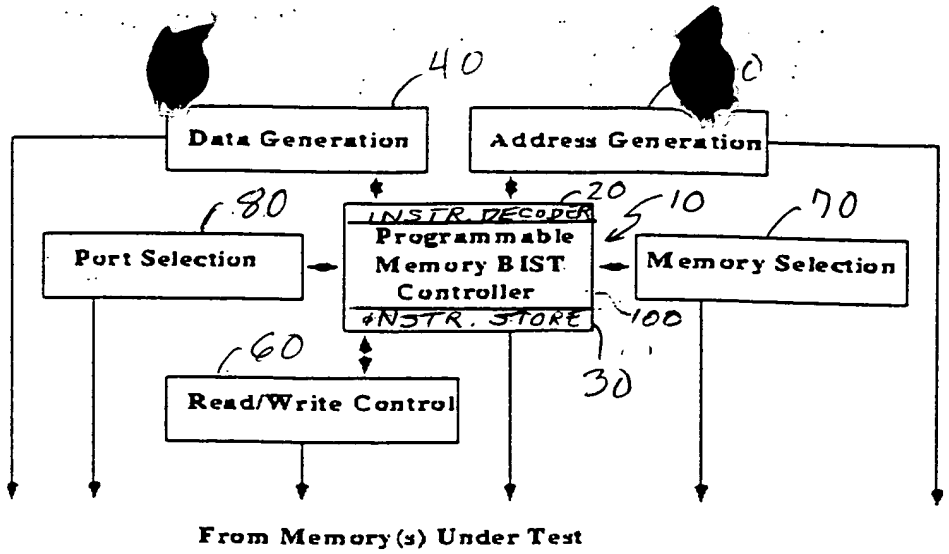

Figure 1. High Level View of a Programmable Memory BIST Module

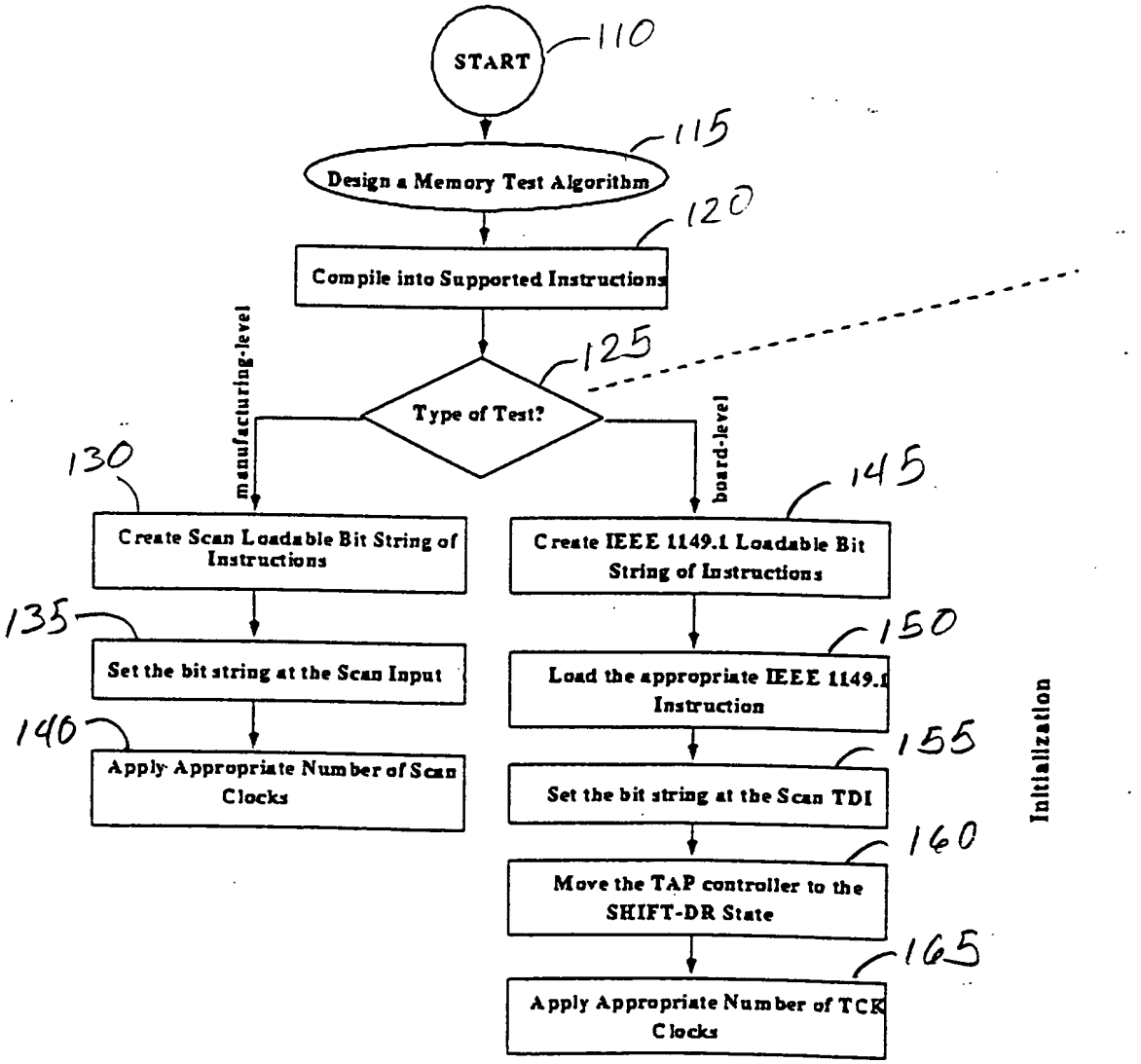

Figure 2. Initialization of Programmable Memory BIST Architecture in Manufacturing-level and Board-level Test

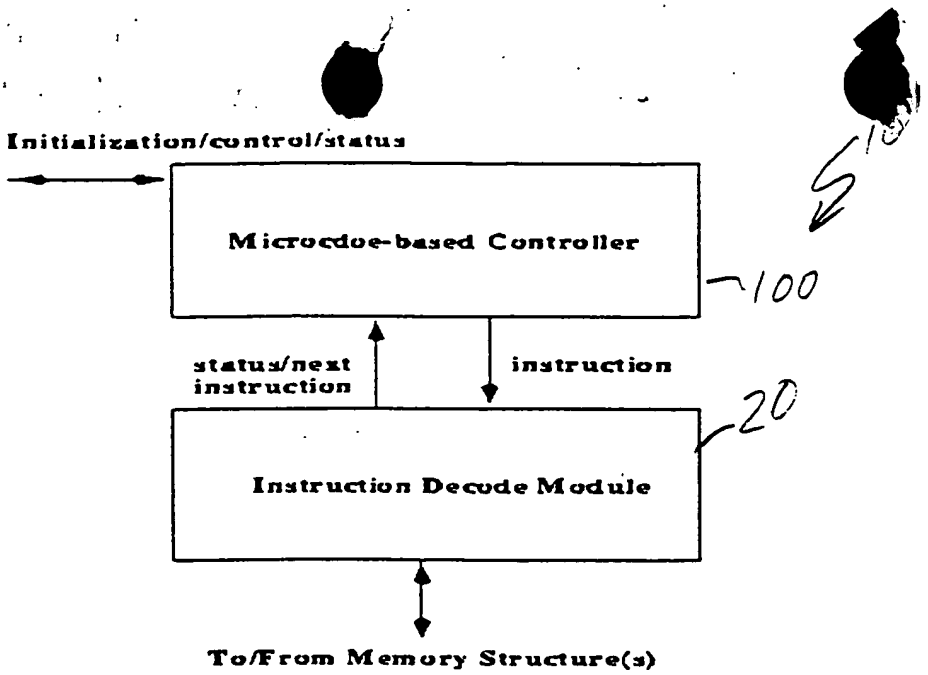

Figure 3. Overview of Programmable Memory BIST Architecture

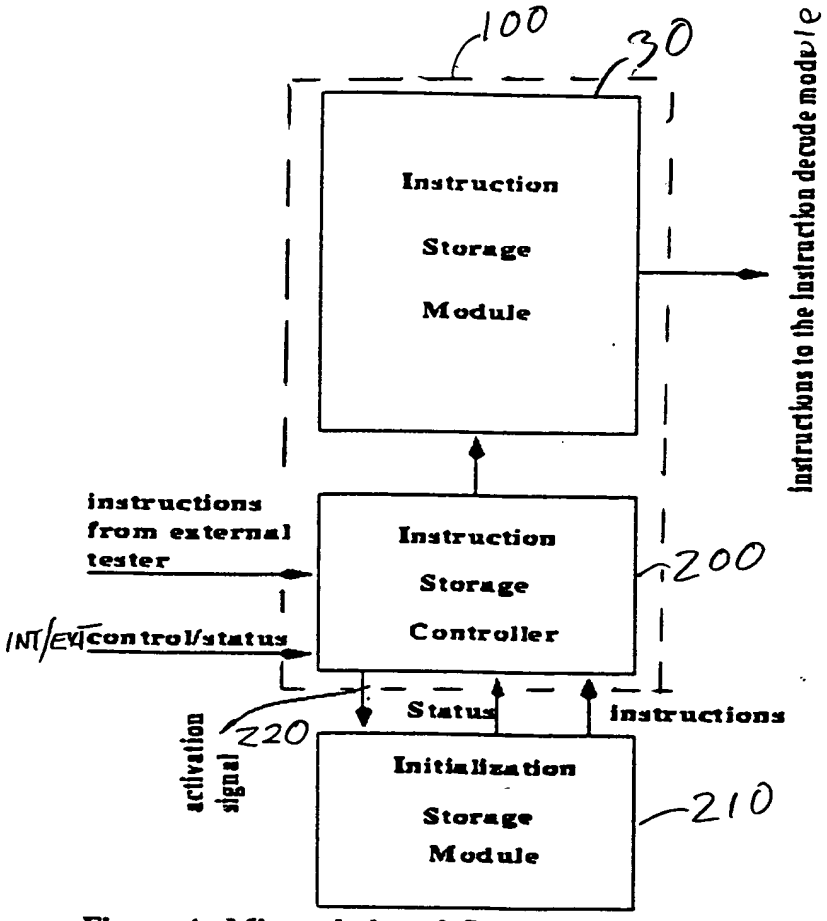

Figure 4. Microcde-based Controller for Programmable Memory BIST Architectures

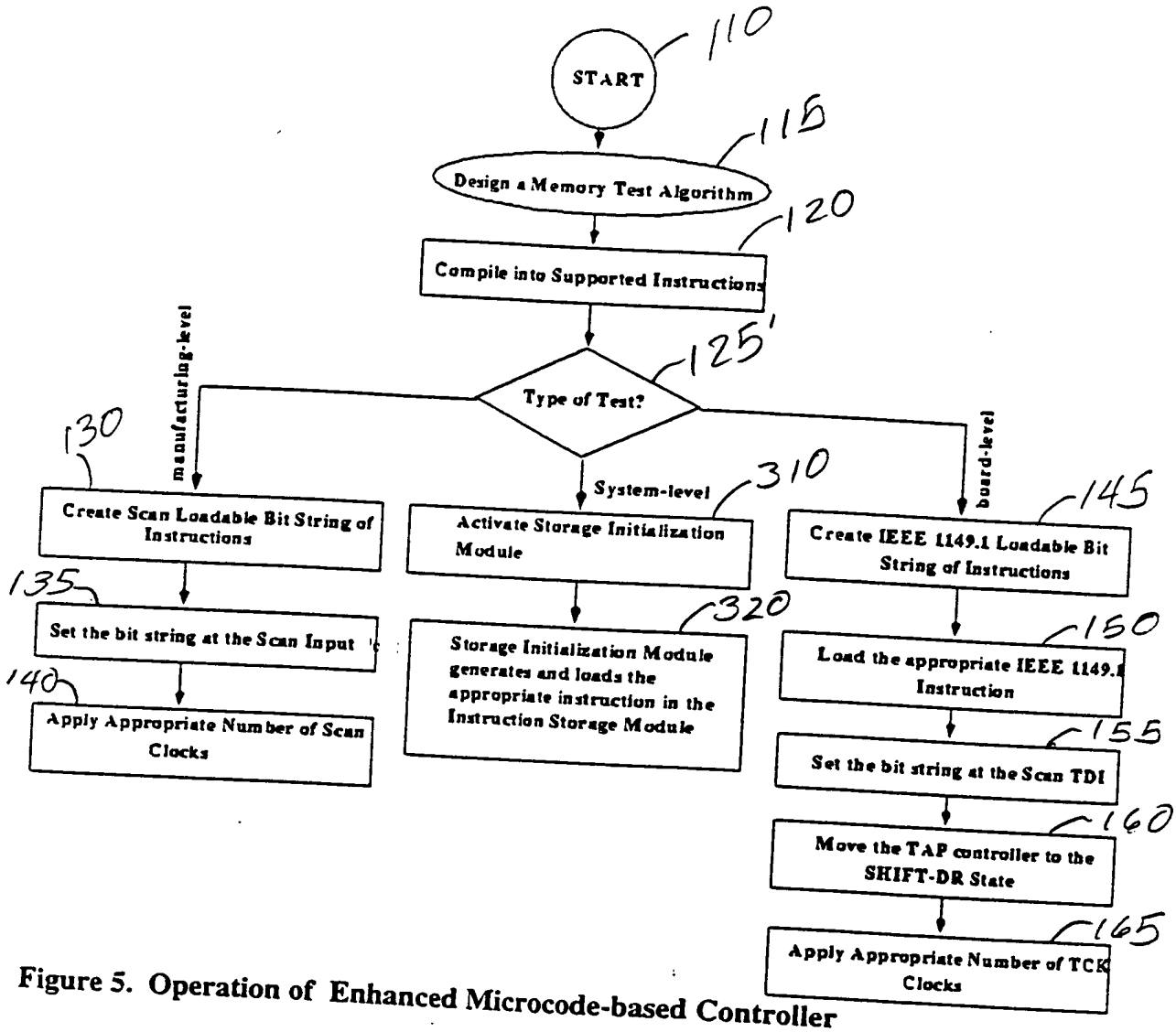

Figure 5. Operation of Enhanced Microcode-based Controller